**AMENDMENTS TO THE CLAIMS:**

Replace the claims with the following rewritten listing:

1. (Currently Amended) Method of establishing an output clock signal (OC) on ~~the~~a basis of an input timing reference (TR), said method comprising: ~~the steps of~~

attenuating jitter of said input timing reference (TR) to produce a control signal ~~(103)~~,

providing at least one intermediate clock signal (IC) on ~~the~~a basis of said control signal ~~(103)~~, at least one of said intermediate clock signals (IC) being justified to a local clock (LC) and being spectrum controlled, and

providing said output clock signal (OC) on ~~the~~a basis of said at least one intermediate clock signal (IC) by attenuating jitter of said at least one intermediate clock signal (IC).

2. (Original) Method of establishing an output clock signal (OC) according to claim 1, whereby at least a part of the jitter of said at least one intermediate clock signal (IC) comprises justification jitter (JJ) originating from said justification to said local clock (LC).

3. (Currently Amended) Method of establishing an output clock signal (OC) according to claim 1 ~~or 2~~, whereby said justification and spectrum control is performed numerically.

4. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims 1 ~~3~~, whereby said attenuation of jitter of said input timing reference (TR) is performed by using low-pass filtering.

5. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims 1~~-4~~, whereby said justification is performed by means of a number-controlled oscillator (NCO).

6. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims ~~1-5~~4, whereby a control input of said number-controlled oscillator (NCO) comprises a period control input.

7. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims 1~~-6~~, whereby said spectrum control comprises dithering.

8. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims 1~~-7~~, whereby said spectrum control comprises noise shaping.

9. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims 1~~-8~~, whereby said local clock (LC) is derived from or comprises a stable reference clock (SC).

10. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims ~~1-9~~, whereby said stable reference clock (SC) comprises a crystal oscillator.

11. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims 1~~-10~~, whereby said local clock (LC) is derived from said output clock signal (OC).

12. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims 1~~-11~~, whereby said attenuation of jitter of said input timing reference (TR) is performed by means of a first block (FBLK), which preferably comprises a time-locked loop, with reference to a stable reference clock (SC).

13. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims 1~~–12~~, whereby at least a part of said justification jitter (JJ) is biased into a higher frequency band.

14. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims 1~~–13~~, whereby said justification jitter (JJ) is low-pass filtered by means of a second block (SBLK), which preferably comprises a phase-locked loop.

15. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims ~~1~~–14, whereby said second block (SBLK) produces a multiplied clock (OEC).

16. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims ~~1~~–15, whereby said second block (SBLK) further produces a frame signal (OFS), said frame signal (OFS) being established by means of frequency division of said multiplied clock (OEC).

17. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims 1~~–16~~, whereby each of said intermediate clock signals (IC) is established by means of at least one numeric stage (FBLK).

18. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims ~~1~~–17, whereby said attenuating jitter of said at least one intermediate clock signal (IC) is performed by means of at least one analog stage (SBLK).

19. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims ~~1~~–18, whereby said at least one analog stage (SBLK) is adapted for attenuating jitter partly or mainly originating from said at least one numeric stage (FBLK).

20. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims 1–~~19~~, whereby each of said intermediate clock signals (IC) is justified to a corresponding local clock (LC) and justification jitter associated with said justification to said local clock is spectrum controlled.

21. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims 1–~~20~~, whereby at least one of said intermediate clock signals (IC) comprises an intermediate event clock component (IEC) and an intermediate framing component (IFS), said intermediate framing being established on ~~the~~a basis of said intermediate event clock by means of frequency division.

22. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims 1–~~21~~, whereby said output clock signal (OC) comprises an output event clock component (OEC) and an output framing component (OFS), said output framing being established on the basis of said output event clock by means of frequency division.

23. (Currently Amended) Method of establishing an event clock (EC) comprising a stream of event-clock pulses (ECP1..ECPn)

on ~~the~~a basis of a master clock (MC) and on ~~the~~a basis of a stream of period control representations (PCR1..PCRn),

the values of said period control representations (PCR1..PCRn) representing ~~the~~a desired period of the event clock (EC) with respect to that of ~~the~~a master clock (MC),

whereby each of said event-clock pulses (ECP1..ECPn) is established on ~~the~~a basis of an associated master-clock pointer (MCP),

in which said master-clock pointers (MCP) form a stream of master-clock pointers (MCP), which stream is derived from said stream of period control representations (PCR1..PCRn) by a process which comprises accumulation and resolution reduction and where an error signal associated with said resolution reduction is spectrum controlled.

24. (Original) Method of establishing an event clock (EC) according to claim 23, whereby said accumulation precedes said resolution reduction.

25. (Currently Amended) Method of establishing an event clock (EC) according to claim 23~~ or 24~~, whereby said resolution reduction precedes said accumulation.

26. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims 23~~-25~~, whereby said resolution reduction may comprise wordlength reduction, quantization, truncation or rounding.

27. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims 23~~-26~~, whereby said event-clock pulses (ECP1..ECPn) are justified to edges of said master clock (MC).

28. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims 23~~-27~~, further comprising:~~ the steps of~~

establishing a representation of an idealized clock comprising a stream of target times (TT) on ~~the~~a basis of period control representations (PCR1..PCRn),

justifying said idealized clock to said master clock (MC) while performing spectrum control of the associated justification jitter,

thereby facilitating number-controlled oscillation with improved control of said justification jitter.

29. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims ~~23~~-28, whereby said period control representations (PCR1..PCRn) are digital.

30. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims ~~23-29~~28, whereby said period control representations (PCR1..PCRn) are analog.

31. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims ~~23-30~~28, whereby said period control representations (PCR1..PCRn) are consecutive components of a discrete-time period control representation signal (PCR).

32. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims 23-~~31~~, whereby said master-clock pointers (MCP) are established on the basis of multiple previous period control representations (PCR1..PCRn).

33. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims 23-~~32~~, whereby said master-clock pointers (MCP) are established on the basis of multiple previous period control representations (PCR1..PCRn) thereby facilitating a continuous accurate establishment of event-clock pulses (ECP1..ECPn).

34. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims 23-~~33~~, whereby said master-clock pointers (MCP) are established on the basis of at least two previous period control representations (PCR1..PCRn) thereby facilitating accurate control of ~~the~~a mean period between consecutive event-clock pulses (ECP1..ECPn).

35. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims 23-~~34~~, whereby said master-clock pointers (MCP) are established on the basis of all previous period control representations (PCR1..PCRn).

36. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims 23-~~35~~, whereby said master-clock pointers (MCP) are established on the basis of integrated period control representations (PCR1..PCRn).

37. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims 23-~~36~~, whereby said master clock (MC) comprises a single-wire clock.

38. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims 23-~~37~~, whereby said master clock (MC) comprises a multiphase clock.

39. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims 23-~~38~~, whereby said master clock (MC) comprises a sequence of master-clock edges.

40. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims ~~23~~-39, whereby a master-clock edge addresser (CR) is synchronized with said master clock (MC), thereby facilitating the selection of those of said master-clock edges that are pointed to by said master-clock pointers (MCP).

41. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims ~~23~~-40, whereby said master-clock edge addresser (CR) comprises a counter (CNT) and a comparator (COM).

42. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims ~~23-41~~40, whereby said master-clock edge addresser (CR) comprises a multiplexer (MPX).

43. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims ~~23-42~~40, whereby said master-clock edge addresser (CR) comprises a differentiator and a multi-modulus divider.

44. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims 23-~~43~~, whereby said period control representations (PCR1..PCRn) are established on the basis of a period control input (PC).

45. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims ~~23-44~~, whereby said period control input (PC) comprises a continuous-time signal.

46. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims ~~23-45~~44, whereby said period control input (PC) comprises an analog signal.

47. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims ~~23-46~~44, whereby said period control representations (PCR1..PCRn) comprise numeric representations of said period control input (PC).

48. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims ~~23-47~~44, whereby said period control representations (PCR1..PCRn) comprise said period control input (PC).

49. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims 23-~~48~~, whereby the process of establishing said master-clock pointers (MCP) comprises quantization.

50. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims ~~23-49~~, whereby the quantization error is subject to spectrum control.

51. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims ~~23~~-50, whereby said spectrum control comprises dithering.

52. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims ~~23-51~~50, whereby said spectrum control comprises noise shaping.

53. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims 23-~~52~~, whereby said spectrum control comprises dithering and noise shaping.

54. (Currently Amended) Method of establishing an event clock (EC) according to ~~any of the~~ claims 23-~~53~~, whereby the resolution of said period control representations (PCR1..PCRn) is greater than the resolution of said master-clock pointers (MCP).

55. (Currently Amended) Clock synchronizer for establishment of an output clock signal (OC) according to ~~any of the~~ claims 1-~~22 or any of the claims 86-90~~.

56. (Currently Amended) Clock synchronizer for establishment of an output clock signal (OC) according to claim 55, further comprising a number-controlled oscillator (NCO)~~ according to any of the claims 23-54~~.

57. (Currently Amended) Clock synchronizer for establishment of an output clock signal (OC) according to claim 55-~~or 56~~, further comprising a circuit for attenuating jitter of an input timing reference (TR), said circuit comprising a number-controlled oscillator (NCO) adapted for establishment of an intermediate clock signal (IC) on the basis of said input timing reference (TR).

58. (Currently Amended) Clock synchronizer for establishment of an output clock signal (OC) according to ~~any of the~~ claims 55-~~57~~, further comprising jitter filtering means (SBLK) adapted for providing said output clock signal (OC) on the basis of said intermediate clock signal (IC).

59. (Currently Amended) Number-controlled oscillator (NCO) comprising means for establishment of an event clock (EC) according to ~~any of the~~ claims ~~23-54~~.

60. (Currently Amended) Method of establishing at least one output signal (CDO) on the basis of at least two input signals (IS1, IS2),
where said input signals each comprise at least
a first component (IS1A, IS2A) and
a second component (IS1B, IS2B) and

where said output signal (CDO) is established fully or partly on ~~the~~a basis of ~~the~~an asynchrony of said first components (IS1A, IS2A) of at least two of said input signals (IS1, IS2) when at least one first predefined criterion is fulfilled and

where said output signal (CDO) is established fully or partly on ~~the~~a basis of ~~the~~an asynchrony of said second components (IS1B, IS2B) of at least two of said input signals (IS1, IS2) when at least one second predefined criterion is fulfilled.

61. (Currently Amended) Method of establishing at least one output signal (CDO) according to claim 60, whereby said at least one output signal (CDO) represents the phase angle between said at least two of said input signals.

62. (Currently Amended) Method of establishing at least one output signal (CDO) according to claim 60 ~~or 61~~, whereby said at least one output signal (CDO) represents the time interval between said at least two of said input signals.

63. (Currently Amended) Method of establishing at least one output signal (CDO) according to ~~any of the~~ claims 60-~~62~~, whereby said input signals (IS1, IS2) are mutually asynchronous.

64. (Currently Amended) Method of establishing at least one output signal (CDO) according to ~~any of the~~ claims 60-~~63~~, whereby said first components (IS1A, IS2A) of said input signals (IS1, IS2) comprise event-clock-representative components.

65. (Currently Amended) Method of establishing at least one output signal (CDO) according to ~~any of the~~ claims 60-~~64~~, whereby said second components (IS1B, IS2B) of said input signals (IS1, IS2) comprise frame-sync-representative components.

66. (Currently Amended) Method of establishing at least one output signal (CDO) according to ~~any of the~~ claims 60-~~65~~, whereby at least one of said input signals (IS1, IS2) comprises feedback signals of a phase-locked loop.

67. (Currently Amended) Method of establishing at least one output signal (CDO) according to ~~any of the~~ claims 60-~~66~~, whereby at least one of said input signals (IS1, IS2) comprises feedback signals of a time-locked loop.

68. (Currently Amended) Method of establishing at least one output signal (CDO) according to ~~any of the~~ claims 60-~~67~~, whereby said first and second components of at least one of said input signals (IS1, IS2) are inherent in a multiphase representation of that signal.

69. (Currently Amended) Method of establishing at least one output signal (CDO) according to ~~any of the~~ claims 60-~~68~~, whereby said first and second components of at least one of said input signals (IS1, IS2) comprise two separately wired signals.

70. (Currently Amended) Method of establishing at least one output signal (CDO) according to ~~any of the~~ claims 60-~~69~~, whereby said first and second components of at least one of said input signals (IS1, IS2) are comprised in a composite signal.

71. (Currently Amended) Method of establishing at least one output signal (CDO) according to ~~any of the~~ claims 60-~~70~~, whereby said first predefined criterion comprises

said asynchrony of said second components (IS1B, IS2B) substantially being smaller than ~~the~~a period of one of said first components (IS1A, IS2A).

72. (Currently Amended) Method of establishing at least one output signal (CDO) according to ~~any of the~~ claims 60~~-71~~, whereby said second predefined criterion comprises said asynchrony of said second components (IS1B, IS2B) substantially exceeding ~~the~~a period of one of said first components (IS1A, IS2A).

73. (Currently Amended) Method of establishing at least one output signal (CDO) according to ~~any of the~~ claims 60~~-72~~, whereby at least one of said predefined criteria is established on ~~the~~a basis of the reliability of at least one of said components (IS1A, IS1B, IS2A, IS2B).

74. (Currently Amended) Method of establishing at least one output signal (CDO) according to ~~any of the~~ claims 60~~-73~~, whereby at least one of said predefined criteria is established on ~~the~~a basis of a quality measure that relates to the performance of a system applying said method.

75. (Currently Amended) Method of establishing at least one output signal (CDO) according to ~~any of the~~ claims 60~~-74~~, whereby said second component (IS1B, IS2B) groups an integer number of clock events of said first components (IS1A, IS2A) into frames and where said number is greater than two.

76. (Currently Amended) Asynchrony detector (CD) comprising means for establishing at least one output signal (CDO) according to ~~any of the~~ claims 60~~-75~~.

77. (Original) Asynchrony detector (CD) according to claim 76, further comprising filtering means (SLF) for filtering said output signal (CDO).

78. (Currently Amended) Asynchrony detector (CD) according to claim 76~~-or 77~~, wherein said output signal (CDO) is used as control signal for an oscillator (VCO).

79. (Currently Amended) Asynchrony detector (CD) according to ~~any of the~~ claims 76-~~78~~, wherein said asynchrony detector forms part of a phase-locked loop.

80. (Currently Amended) Asynchrony detector (CD) according to ~~any of the~~ claims 76-~~79~~, wherein said asynchrony detector forms part of a time-locked loop.

81. (Currently Amended) Asynchrony detector (CD) according to ~~any of the~~ claims 76-~~80~~, wherein said output signal (CDO) is established by means of

at least two synchronous state machines (RSSM, FSSM), each acting on one of said input signals (IS1, IS2) and on at least one signal from at least one other of said synchronous state machines (RSSM, FSSM),

at least one frame offset counter (FOC),

at least one combinatorial block (CMB) adapted to process event count values derived from said synchronous state machines (RSSM, FSSM) and to process force signals (FUP, FDN) derived from said frame offset counter (FOC).

82. (Currently Amended) Asynchrony detector (CD) according to ~~any of the~~ claims 76-~~81~~, wherein said output signal (CDO) is established by means of a set of at least two basic asynchrony detectors (DET1, DET2, DET3, DETn), said set of detectors being adapted to act on multiphase clocks (MPIC, MPFC).

83. (Currently Amended) Asynchrony detector (CD) according to ~~any of the~~ claims ~~76~~-82, wherein at least one of said multiphase clocks (MPIC, MPFC) is established by means of a divider (RDIV, FDIV).

84. (Currently Amended) Asynchrony detector (CD) according to ~~any of the~~ claims 76-~~83~~, wherein said at least one output signal (CDO) is established by means of at least one counter (RCTR, FCTR) and a digital-to-analog converter (DAC).

85. (Currently Amended) Asynchrony detector (CD) according to ~~any of the~~ claims 76~~-84~~, wherein ~~said at least one output signal (CDO) is established by means of combining the asynchrony detector of claim 82 or 83 with the asynchrony detector of claim 84.~~said output signal (CDO) is established by means of a set of at least two basic asynchrony detectors (DET1, DET2, DET3, DETn), said set of detectors being adapted to act on multiphase clocks (MPIC, MPFC) and wherein said at least one output signal (CDO) is established by means of at least one counter (RCTR, FCTR) and a digital-to-analog converter (DAC).

86. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims 1~~-22~~, whereby said justification is performed by means of a number-controlled oscillator (NCO) according to claim 59.

87. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims ~~1-22 or 86~~14, whereby said second block (SBLK) comprises an asynchrony detector (CD)~~ according to any of the claims 76 to 85~~.

88. (Currently Amended) Method of establishing an output clock signal (OC) according to any of the claims 1~~-22 or any of the claims 86-87~~, whereby said output clock signal (OC) is phase locked to said input timing reference (TR).

89. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims 1~~-22 or any of the claims 86-88~~, whereby said output clock signal (OC) is frequency locked to said input timing reference (TR).

90. (Currently Amended) Method of establishing an output clock signal (OC) according to ~~any of the~~ claims 1~~-22 or any of the claims 86-89~~, whereby said output clock signal (OC) is frequency ratio locked to said input timing reference (TR).